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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,415	04/12/2004	David Walker Guidry	TI-37398	2557

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EXAMINER	
SIDDIQUI, SAQIB JAVAID	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,415	GUIDRY, DAVID WALKER	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/22/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *2,3 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-16 and 18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered August 22, 2006.

- Claims 1-21 are pending.
- Claims 1, 7-8, 13, 16 & 18 are amended.
- Claims 2-3 & 17 are canceled
- Application is currently pending.

Response to Amendment

Applicant's arguments and amendments with respect to claims 1-21 filed August 22, 2006 have been fully considered but they are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends that the prior arts of record do not teach a multiplexer for interfacing the DUT with an automatic test equipment (ATE) operably connected to perform testing on the DUT. Examiner respectfully disagrees.

As per US Pat no. 5,701,309, Gearhardt et al. mentions "Boundary scan implementations such as those shown in the aforementioned IEEE Standard 1149.1 include a multiplexer circuit which allows the IC to select either a boundary scan input signal or the conventional data signal which is supplied to the IC from the normal data source. In this manner, an IC equipped for boundary scan may be used in either a test mode or a normal operative mode. Digital testers which are referred to generically as automated test equipment (ATE) actually perform the IC testing described above. It

will be appreciated that in order for such ATE to perform scan-based testing of an IC, the IC or device under test (DUT) must of course be a scan-based logic design specifically designed to permit such testing as per the IEEE 1149.1 standard or other custom-designed scan logic implementation. Such an IC (or DUT) is depicted being tested by an ATE device in FIG. 1." (columns 1-2, lines 60-10). Here clearly, the IEEE Standard 1149.1 is used in deigning the aforementioned ATE, where the ATE chooses to test the DUT and the ATE includes a multiplexer, used to chose between a test mode or scan mode.

As per US Pat no. 6,675,339 B1 Lanier et al. mentions "Multiplexers 714, 716, and 718 each have inputs coupled to device under test 50... Sequenced measure system 610 performs the sequence source and measure analog tests with respect to device under test 50. Sequenced measure system 610 is coupled to DUT 50. Sequenced measure system 610 includes a source circuitry 820 and measure circuitry 818. Source circuitry 820 includes multiplexer 714, divider 720, source sequencer 726, sequencer memory 728, source waveform memory 734, and event processor 710." (Fig 22, columns 29-30, lines 5-30). Here clearly, the sequence measure circuit performs the testing on the DUT, and the circuitry is connected to the DUT by multiplexers, as clearly seen in Figure 22.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-21 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Gearhardt et al. US Patent no. 5,701,309.

As per claim 1:

Gearhardt et al. teaches for testing semiconductor devices, a digital testing system (Figure 2) comprising: a testing module (Figure 3) including: pattern memory for storing test vectors adapted for performing digital tests (Figure 2, # 80, column 5, lines 1-55); a digital test engine for implementing test vectors of the pattern memory (Figure 2 # 25), whereby digital inputs are provided to a device under test (DUT) (Figure 2 # 70) and digital DUT outputs are captured (Figure 2 # 70), thereby testing the operability of the DUT (Figure 2 # 30) and a multiplexer for interfacing the DUT with automatic test equipment (ATE) (column 1, lines 40-67); and ATE operably connected to perform testing on the DUT (Figure 2 # 25, column 4, 25-37).

As per claim 5:

Gearhardt et al. teaches the digital testing system as rejected in claim 1, configured to perform scan testing (Figure 2, # 10).

As per claim 6:

Gearhardt et al. teaches the digital testing system as rejected in claim 1, configured to perform functionality testing (column 6, lines 50-58).

As per claim 7:

Gearhardt et al. teaches the digital testing system as rejected in claim 1, wherein the testing module comprises a hardware device (Figure 2 # 30).

As per claim 8:

Gearhardt et al. teaches the digital testing system as rejected in claim 1, wherein the testing module comprises firmware (Figure 2 # 27).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gearhardt et al. US Patent no. 5,701,309 and further in view of Lanier et al. US Patent no. 6,675,339 B1.

As per claim 4:

Gearhardt et al. substantially teaches a digital testing system (Figure 2) comprising: pattern memory for storing test vectors adapted for performing digital tests

(Figure 2, # 80, column 5, lines 1-55); a digital test engine for implementing test vectors of the pattern memory (Figure 2 # 25), whereby digital inputs are provided to a device under test (DUT) (Figure 2 # 70) and digital DUT outputs are captured (Figure 2 # 70), thereby testing the operability of the DUT (Figure 2 # 30).

Gearhardt et al. does not explicitly teach the system configured to perform mixed signal testing.

However Lanier et al. in an analogous art teaches a digital testing system configured to perform mixed signal testing (Abstract, lines 1-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made enable the ATE in Gearhardt et al's invention to be able to generate mixed test signals, since one of ordinary skill in the art would have realized that enabling Gearhardt et al.'s invention to generate mixed test signals would have provided it the ability to test DUT's with different configurations and specifications, hence making their invention more encompassing.

Claims 9, & 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lanier et al. US Patent no. 6,675,339 B1.

As per claim 9:

Lanier et al. substantially teaches a digital testing system for adding digital test capability to an automatic test equipment (ATE) platform (Figure 1 # 20), the system comprising; automatic test equipment (ATE) adapted for performing analog testing of a device under test (DUT) (column 4, lines 25-35); and a testing module further comprising pattern memory (Figure 1 # 674), a test engine (Figure 1 # 20), and a

multiplexer for interfacing the DUT with the ATE (Figure 22 # 714, column 29, lines 1-15), for performing digital testing on the DUT (Figure 1 # 50).

Lanier et al. discloses the claimed invention except for the location of the multiplexer. It would have been obvious to one having ordinary skill in the art at the time the invention was made incorporate the multiplexer within the ATE, since it has been held that rearranging parts of an invention involves only routine skill in the art. In *re Japikse, 86 USPQ 70.* Further it should be noted that claim 9 can be rejected under 102(e), since claim 9 does not disclose any location of the multiplexer, however examiner is giving a 103 keeping in consideration the location of the multiplexer in the invention.

As per claim 12:

Lanier et al. teaches the digital testing system as rejected in claim 9 above wherein the testing further comprises a high speed bus (Figure 3 # 94, column 8, lines 30-60).

As per claim 13:

Lanier et al. teaches the digital testing system as rejected in claim 9 above configured to perform scan mixed signal device testing (Abstract, lines 1-10).

As per claim 14:

Lanier et al. teaches the digital testing system as rejected in claim 9 above configured to perform scan testing (column 4, lines 24-65).

As per claim 15:

Lanier et al. teaches the digital testing system as rejected in claim 9 above configured to perform functionality testing (Figure 6 # 187, column 12, lines 20-40).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lanier et al. US Patent no. 6,675,339 B1 and further in view of Gearhardt et al. US Patent no. 5,701,309.

As per claim 10:

Lanier et al. teaches the digital testing system as rejected in claim 9 above.

Lanier et al. does not explicitly teach the digital testing system wherein the testing module further comprises DDR SRAM.

However, Gearhardt et al. in an analogous art teaches a digital testing system wherein the testing module further comprises DDR SRAM (Figure 2 # 80). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the DDR SRAM in the testing module, since one of ordinary skill in the art would have realized that enabling Lanier et al.'s invention to use the DDR SRAM in the invention would have accounted for higher speeds and lower power consumptions. Further it should be noted that Lanier et al. does not point out the kind of memory being used in the invention, which might even be the DDR SRAM.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lanier et al. US Patent no. 6,675,339 B1 and further in view of Sabih et al. US Patent no. 6,904,375 B1.

Lanier et al. teaches the digital testing system as rejected in claim 9 above.

Lanier et al. does not explicitly teach the digital testing system wherein the testing module further comprises an FPGA.

However, Sabih et al. in an analogous art teaches a digital testing system wherein the testing module further comprises an FPGA (column 2, lines 45-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an FPGA in the testing module, since one of ordinary skill in the art would have realized that enabling Lanier et al.'s invention to use an FPGA in the invention eliminates or reduces the need for an instruction-based processor and eliminate the need for custom ASIC processing functions.

As per claims 16-21:

Claims 16-21 are directed to a method of the system of Claims 1-15. Gearhardt et al., Sabih et al. and Lanier et al., either alone or in combination as stated above, the system as set forth in Claims 1-4. Therefore, Gearhardt et al., Sabih et al. and Lanier et al. also teach, either alone or in combination as stated above, the method as set forth in Claims 16-21, wherein the device interface board is represented in Figure 2 # 25, Gearhardt et al. and Figure 1 # 16, Lanier et al.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Examiner's Note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

Saqib Siddiqui
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11/03/2006

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